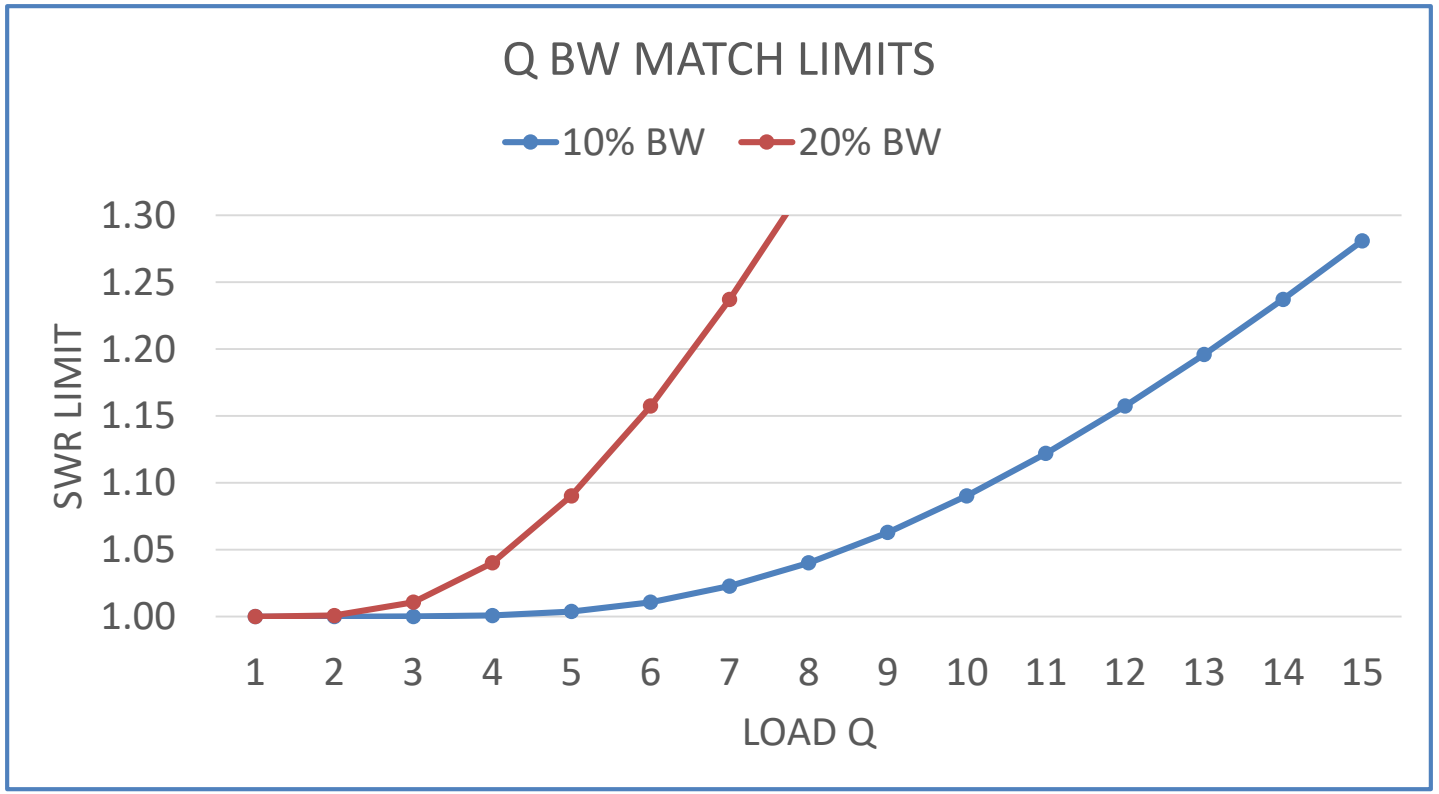
IMPEDANCE MATCHING TECHNIQUES FOR RF & MICROWAVE CIRCUIT DESIGN

2019 Microwave Update

ACHIEVABLE MATCH DEPENDS ON Q_L AND BW%

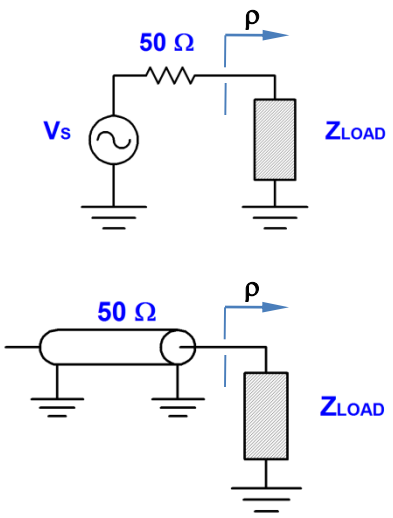


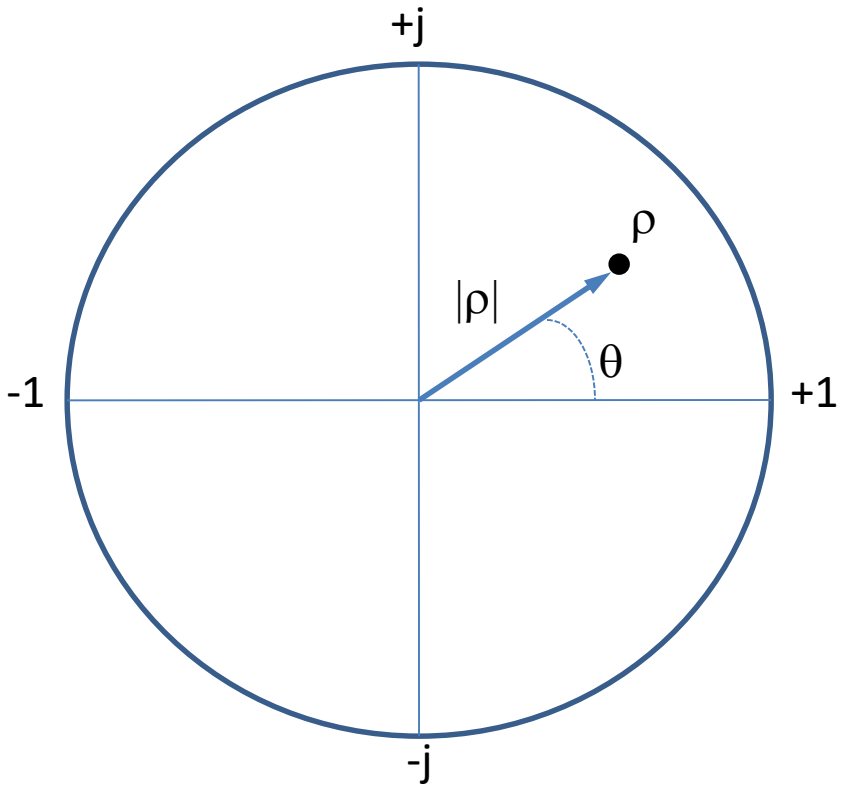
$$\rho \geq e^{\left(\frac{-\pi}{Q*BW}\right)}$$

$$SWR = (1+\rho)/(1-\rho)$$

ORIGIN OF THE SMITH CHART

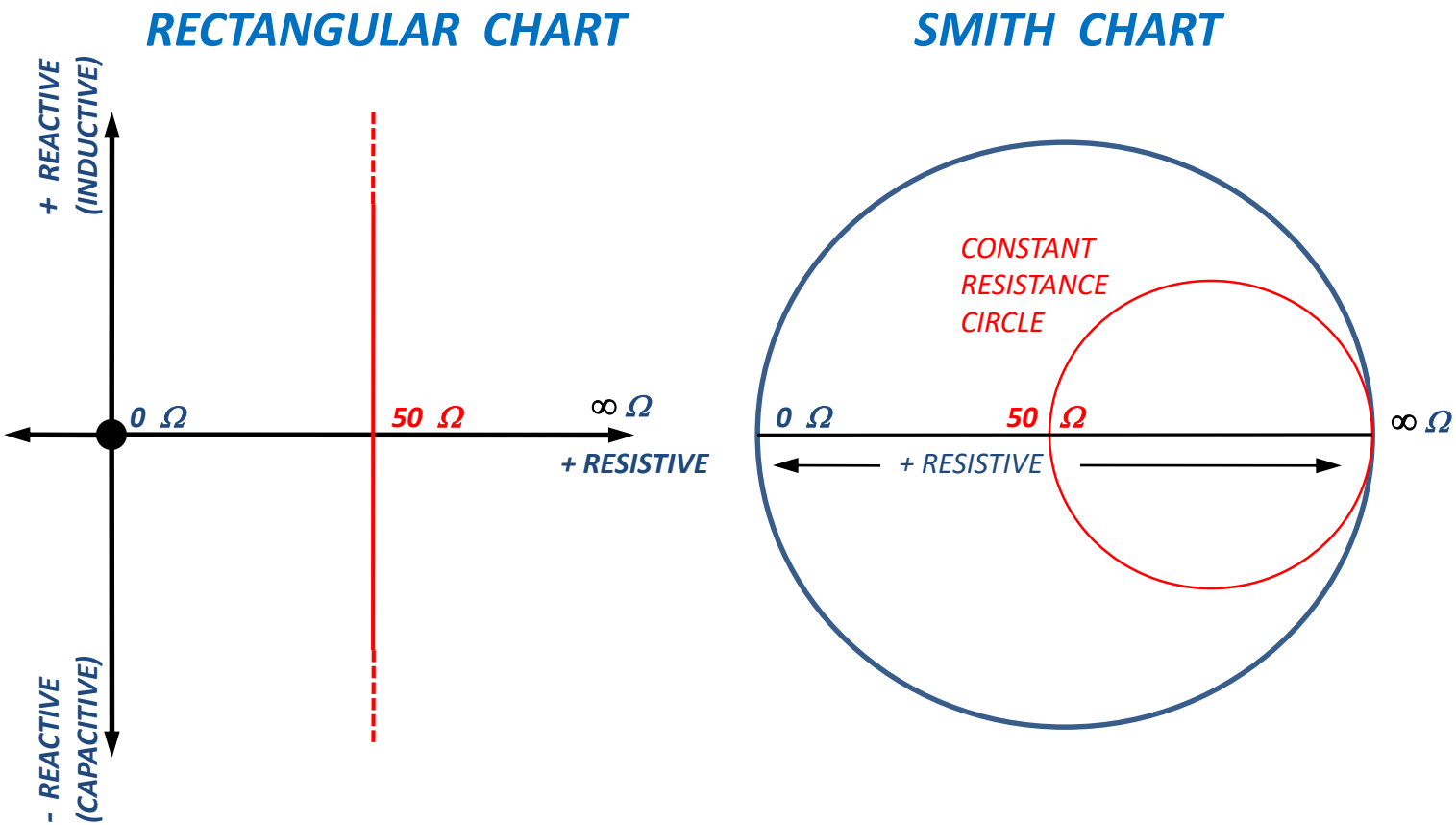
REFLECTION COEFFICIENT: ρ





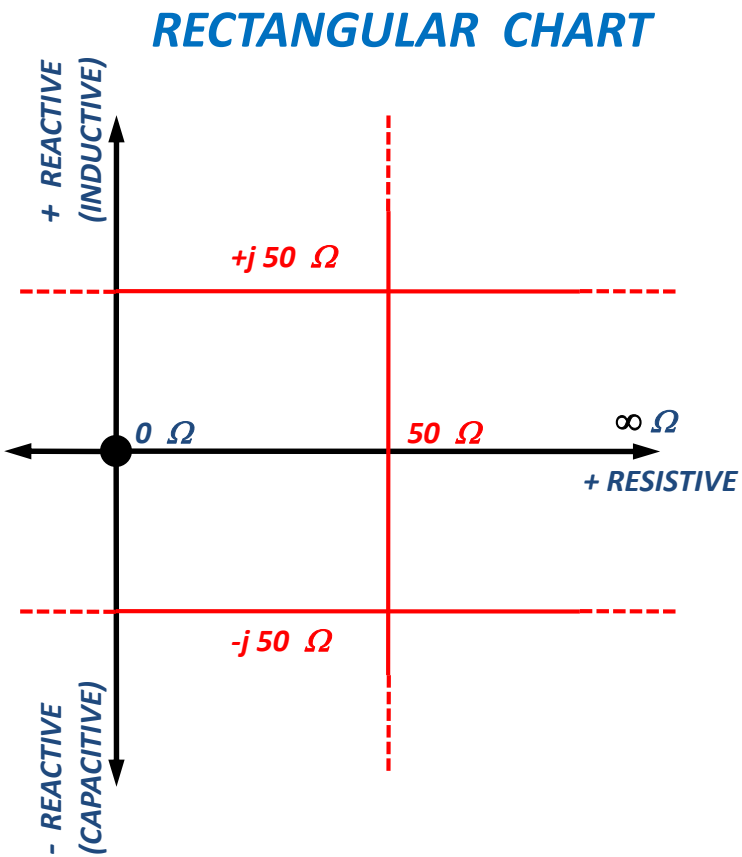
- ρ IS RATIO OF REFLECTED TO FORWARD VOLTAGE AT LOAD
- ρ IS COMPLEX NUMBER: (REAL, IMAGINARY) or (MAGNITUDE, ANGLE)
- |ρ| =1.0 IS MAXIMUM POSSIBLE WITH PASSIVE LOAD (TOTAL REFLECTION)
- |ρ| =1.0 CIRCLE IS OUTER BOUNDARY OF STANDARD SMITH CHART

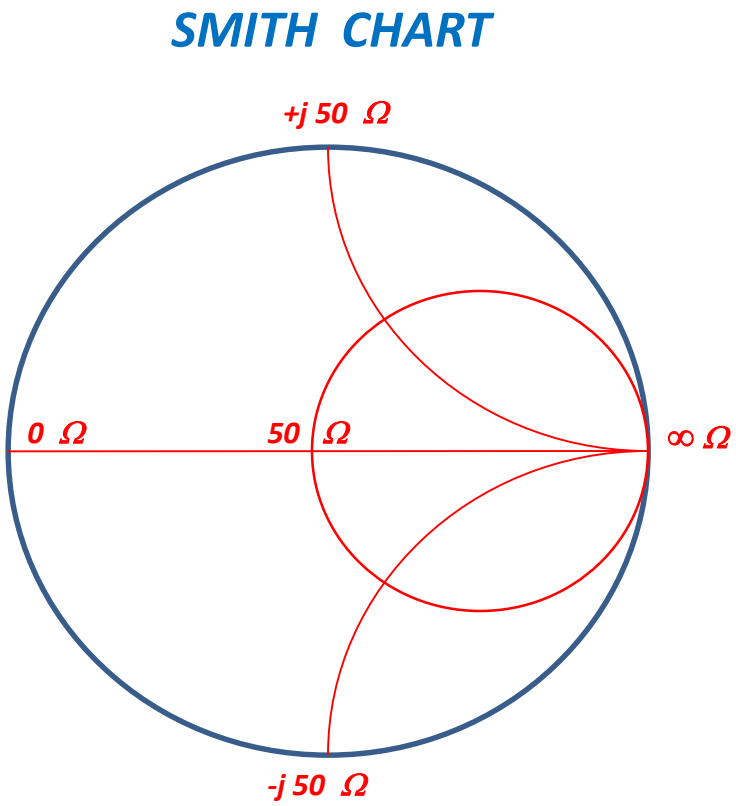
IMPEDANCE VIEW – CONSTANT RESISTANCE



- **Z = R + j X**
- IMPEDANCE HAS A REAL PART AND AN IMAGINARY PART
- IMPEDANCE REPRESENTS A SERIES CONNECTION
- CONSTANT REAL LINES BECOME CIRCLES ON SMITH CHART

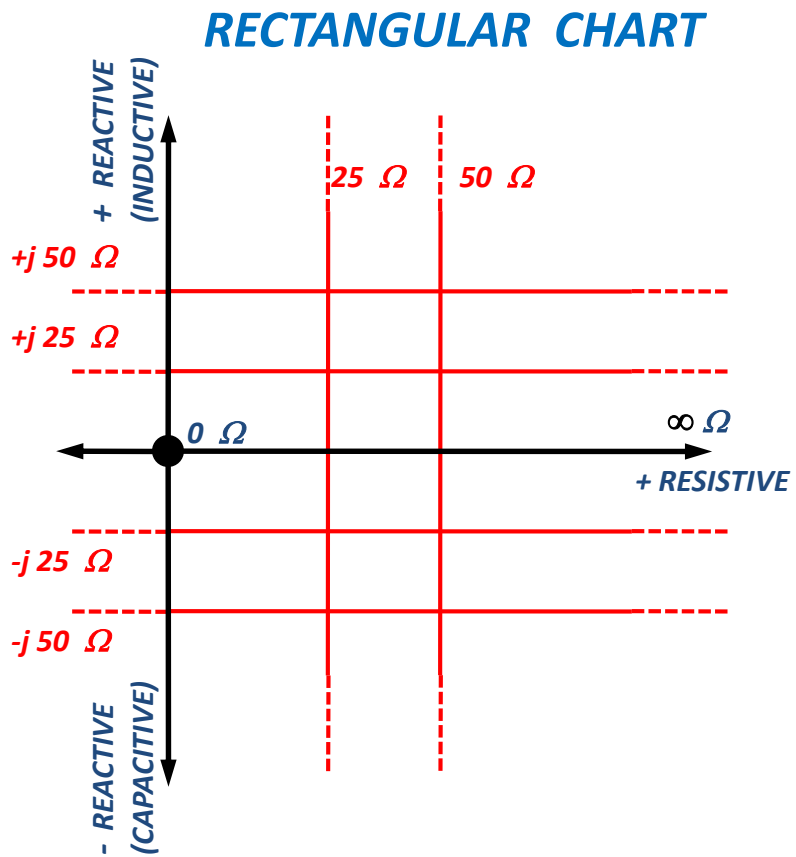
IMPEDANCE VIEW – CONSTANT REACTANCE

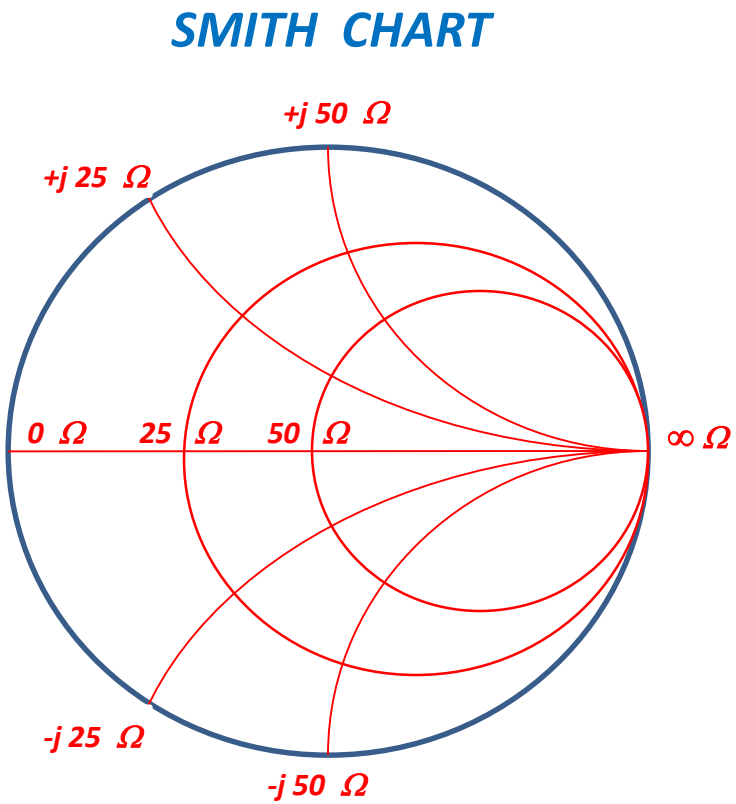




- CONSTANT REACTANCE LINES BECOME ARCS ON SMITH CHART
- UPPER HALF IS INDUCTIVE
- LOWER HALF IS CAPACITIVE
- POSITIVE REAL IS INSIDE THE SMITH UNIT CIRCLE

IMPEDANCE VIEW

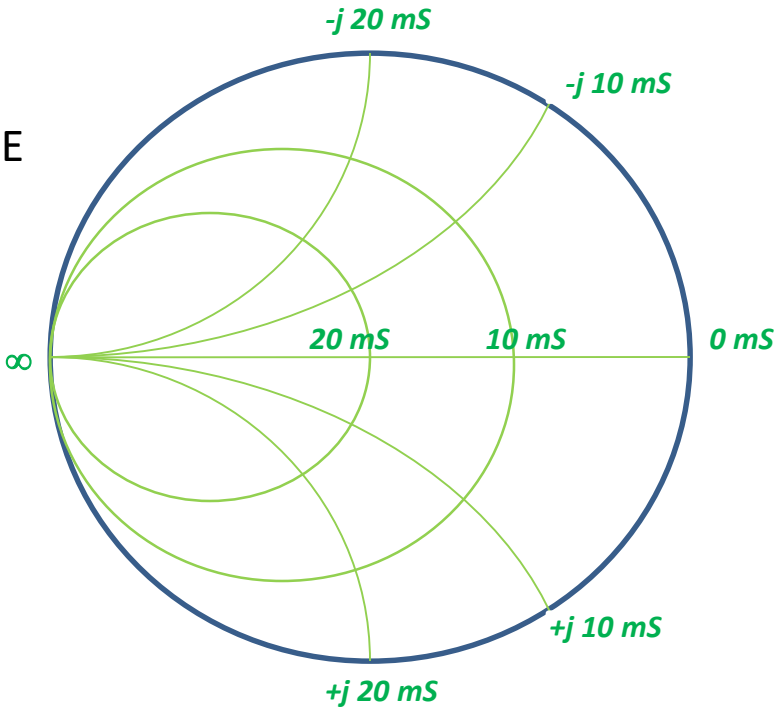




- IMPEDANCE REPRESENTATION OF THE SMITH CHART
- USUALLY IN RED
- LOWER HALF IS CAPACITIVE
- POSITIVE REAL IS INSIDE THE SMITH UNIT CIRCLE

ADMITTANCE VIEW

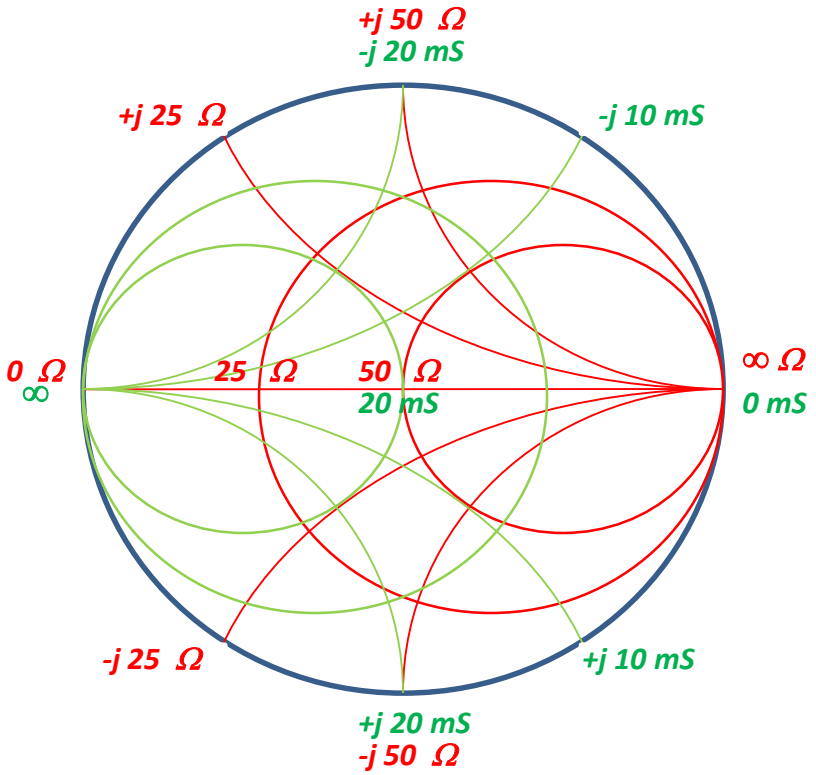
- **Y = 1/Z = G + j B**
- ADMITANCE IS RECIPROCAL IMPEDANCE
- ADMITANCE REPRESENTS A PARALLEL CONNECTION



- ADMITANCE HAS A REAL PART (CONDUCTANCE) AND AN IMAGINARY PART (SUSCEPTANCE)
- CONSTANT CONDUCTANCE IS A CIRCLE ON SMITH CHART
- CONSTANT SUSCEPTANCE IS AN ARC ON SMITH CHART

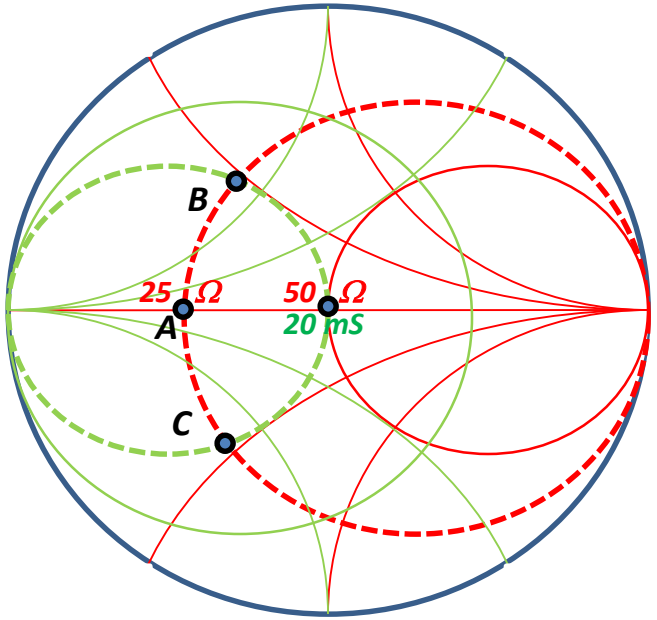
OVERLAY SMITH CHART

- BOTH IMPEDANCE AND ADMITANCE VIEWS OF SAME POINT
- SIMULTANEOUS VIEW OF SERIES IMPEDANCE OR PARALLEL ADMITTANCE
- THIS VIEW PROVIDES A CONVENIENT WAY TO DESIGN LUMPED ELEMENT MATCHING NETWORKS
- DOWNLOAD A NORMALIZED CHART:
  http://k5tra.net/TechFiles/smith_color.pdf



LUMPED ELEMENT Z-MATCHING

- A SIMPLE EXAMPLE IS TO MATCH BETWEEN 25 Ω AND 50 Ω
- FROM THE 25 Ω POINT (***A)*** WE FIRST USE THE IMPEDANCE VIEW TO MOVE TO EITHER POINT ***B*** OR ***C***
- ***A***, ***B***, and ***B*** ARE ALL ON THE CONSTANT 25 Ω CIRCLE
- THE (+) REACTIVE SHIFT FROM ***A*** TO ***B*** REPRESENTS A SERIES INDUCTOR
- THE (-) REACTIVE SHIFT FROM ***A*** TO ***C*** REPRESENTS A SERIES CAPACITOR
- NOTE THAT BOTH ***B*** and ***C*** ARE ON THE 20 mS CIRCLE. THIS ALLOWS US TO REACH 50 Ω WITH A SHUNT ELEMENT



- THROUGH ***B*** REQUIRES SERIES INDUCTOR AND SHUNT CAPACITOR
- THROUGH ***C*** REQUIRES SERIES CAPACITOR AND SHUNT INDUCTOR

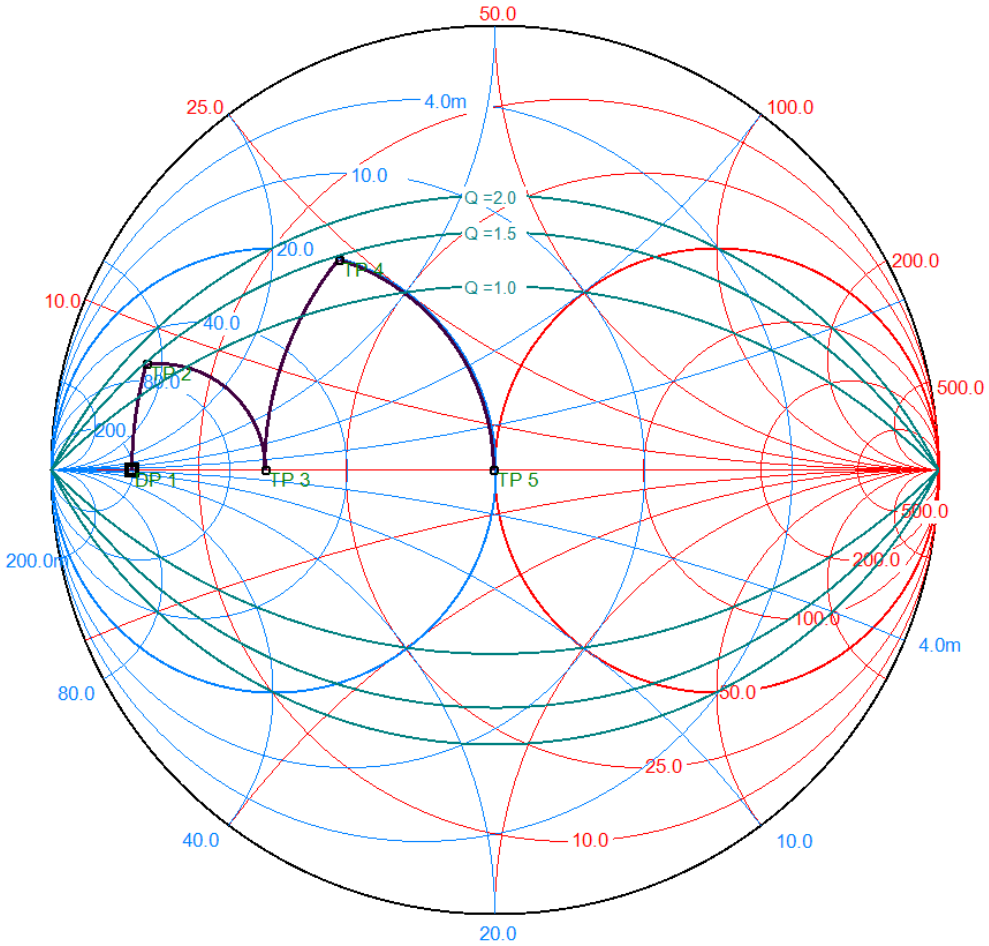
L OR C VALUES FROM CHART

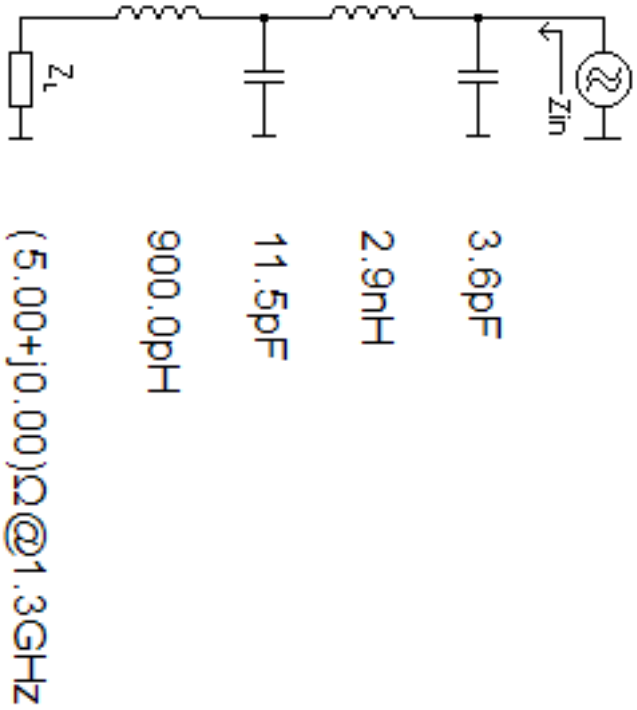
- SERIES L OR C ELEMENT VALUES ARE CALCULATED FROM REACTANCE SHIFTS ALONG A CONSTANT RESISTANCE CIRCLE:
- $L_S = \frac{|X_L|}{2\pi F}$ and $C_S = \frac{1000}{2\pi F|X_C|}$,

  units are L(nH), C(pF), X(Ω) and F(GHz).
- SHUNT L OR C ELEMENT VALUES ARE CALCULATED FROM SUSCEPTANCE SHIFT ALONG A CONSTANT CONDUCTANCE CIRCLE:
- $C_P = \frac{|B_C|}{2\pi F}$ and $L_P = \frac{1000}{2\pi F|B_L|}$,

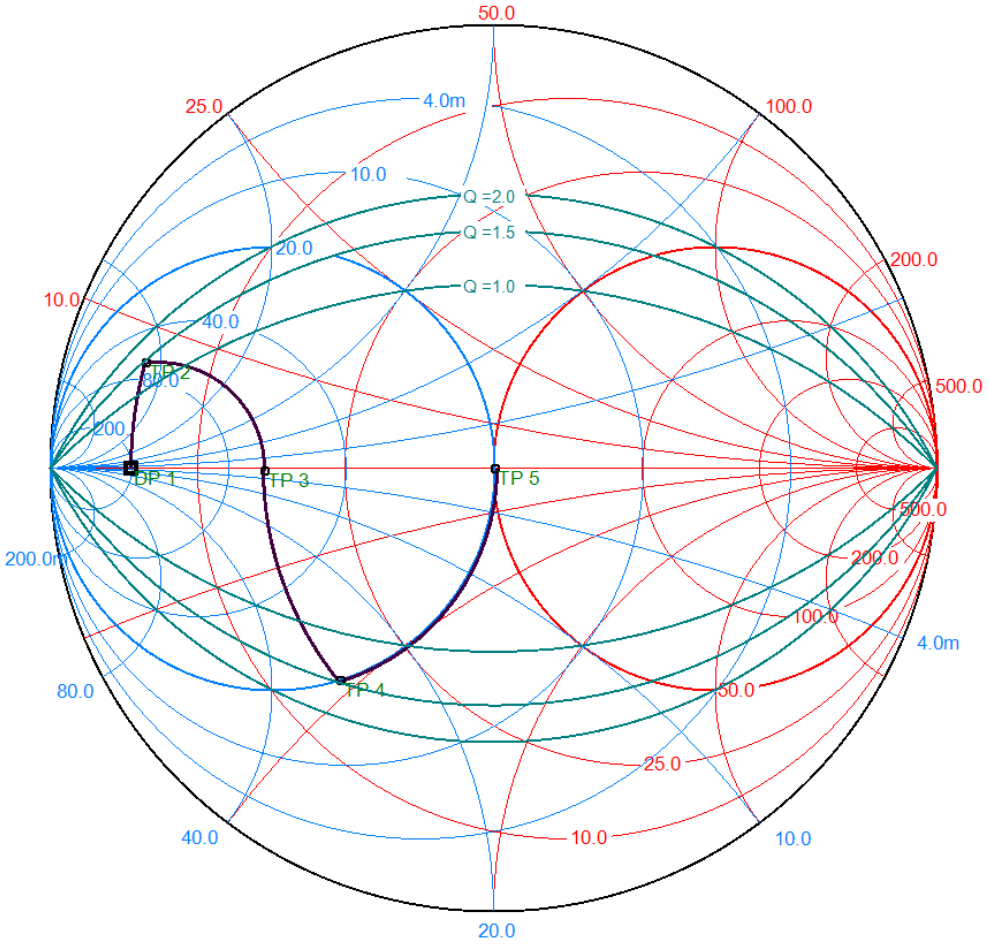
  units are L(nH), C(pF), B(mS) and F(GHz).

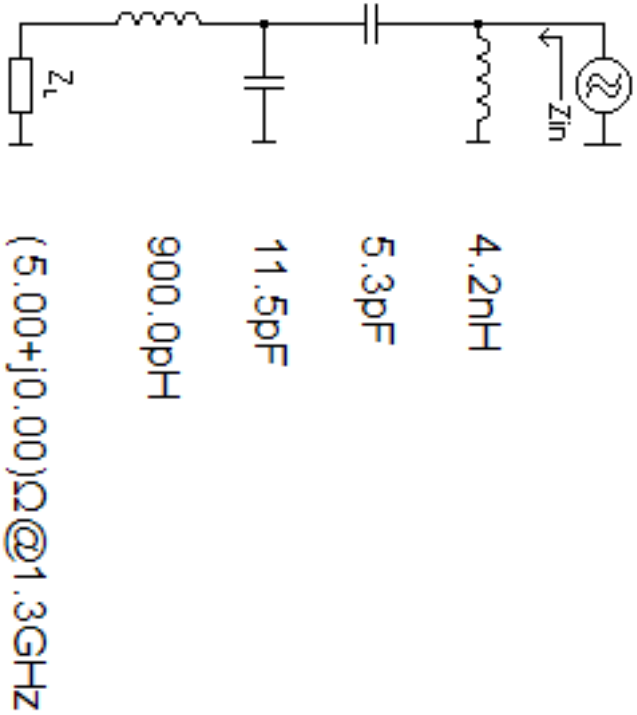
Ls Cp Ls Cp LOWPASS MATCH



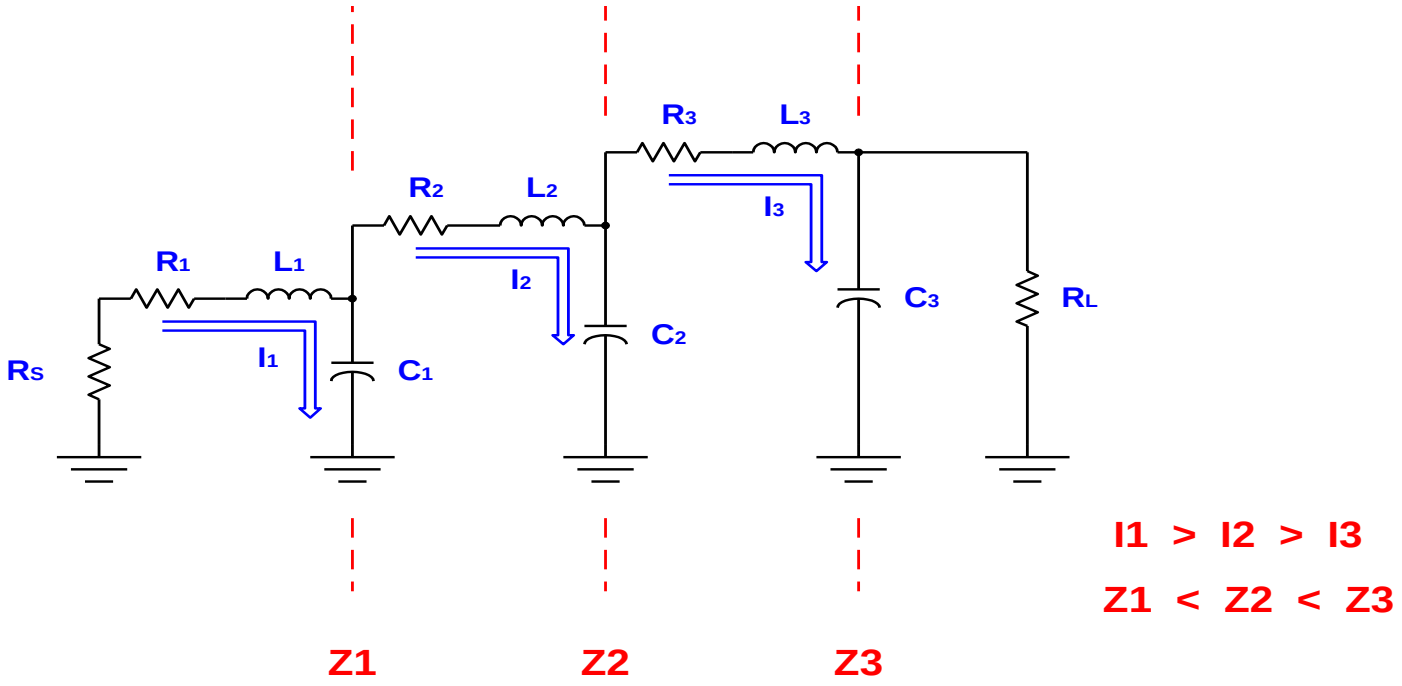


Ls Cp Cs Lp BANDPASS MATCH



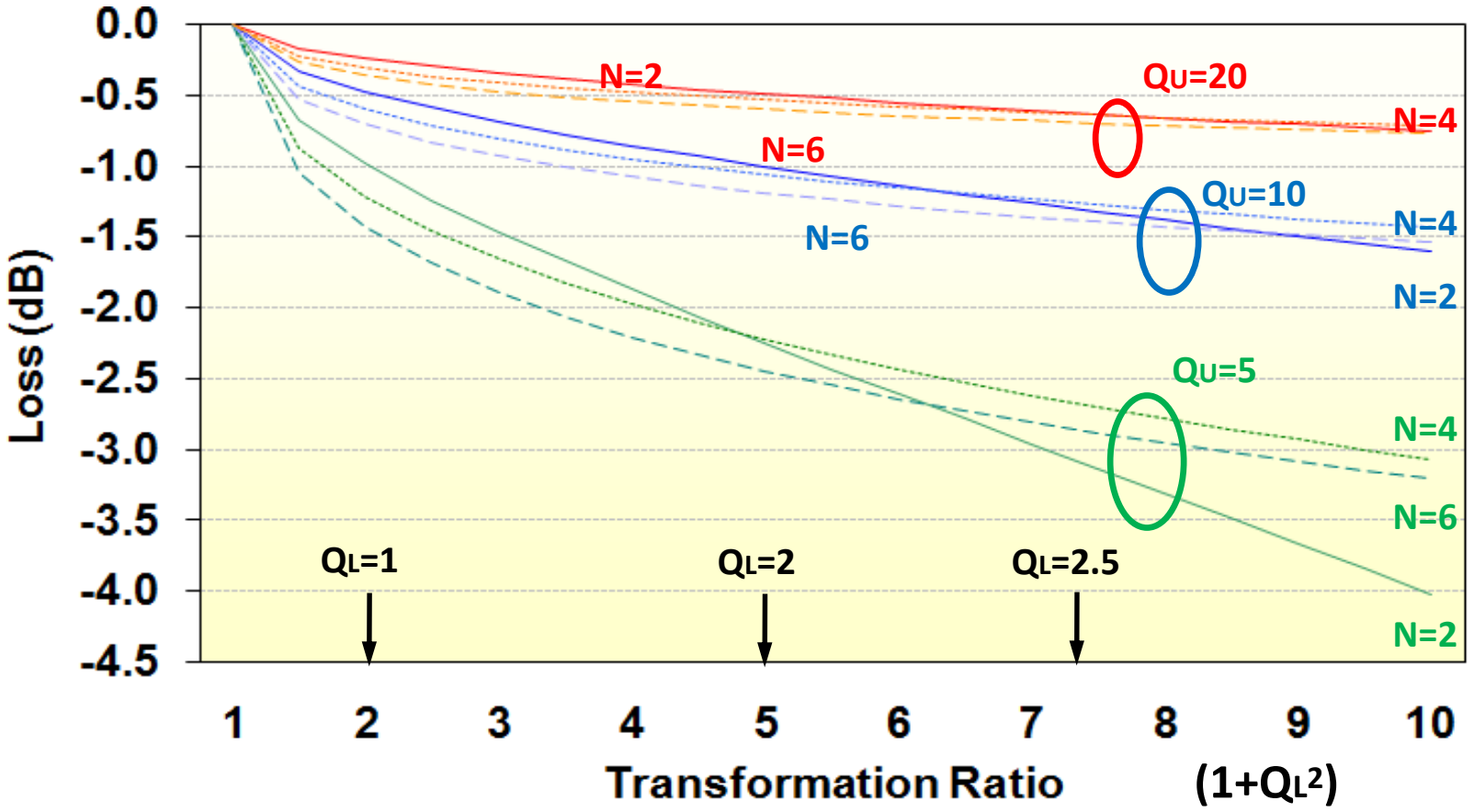


LOSS CONSIDERATIONS



- POWER TRANSFER OF EACH SECTION IS: $(Q_U - Q_L) / Q_U$
- I^2 R LOSSES (PRIMARILY IN INDUCTORS) PRODUCE INSERTION LOSS
- Z TRANSFORMATION PER SECTION IS: $1 + Q_L^2$
- IMPEDANCE TRANSFORMATION REQUIRES: $QL > 1$

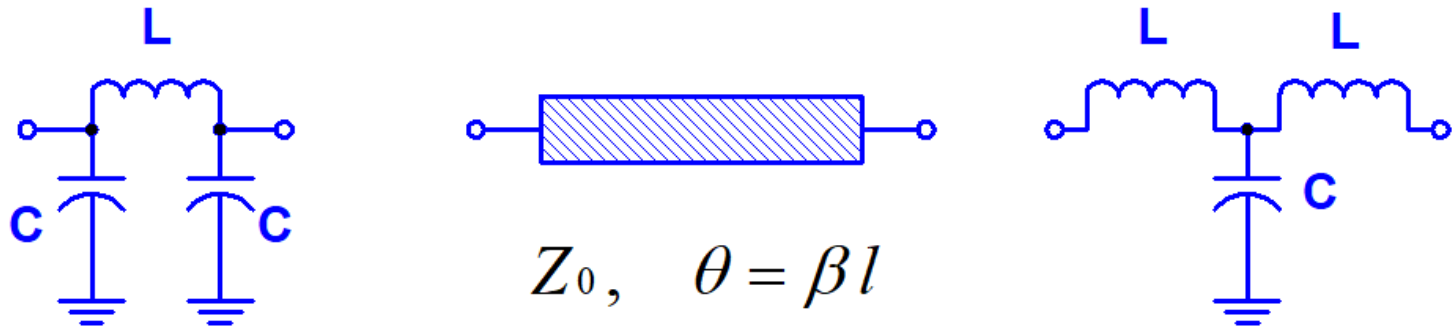
NUMBER OF ELEMENTS - LOSS TRADE-OFF



LUMPED DESIGN ON A CIRCUIT BOARD

- THERE REALLY ARE NO LUMPED ELEMENTS
  - CHIP CAPACITORS HAVE SERIES INDUCTANCE (and LOSS)
  - CHIP INDUCTORS HAVE DISTRUBUTED CAPACITNCE (SELF RESONANCE)
  - CHIP RESISTORS HAVE SERIES INDUCTANCE AND SHUNT CAPACITANCE
- CIRCUIT BOARD TRACES OVER BACKSIDE GROUND ARE MICROSTRIP TRANSMISSION LINES.
- MICROSTRIP LINES ARE QUASI-TEM; SO THEY CAN BE REPRESENTED AS A SERIES OF INCREMENTAL SERIES L AND SHUNT C ELEMENTS.
- $Z_0 = \sqrt{\frac{L}{C}}$, WHERE L AND C ARE INCREMENTAL (PER UNIT LENGTH)
- THIN TRACES:
  - HIGH Zo TRACES HAVE HIGH L/C
  - USED FOR PRINTED INDUCTORS
- WIDE TRACES:
  - LOW Zo TRACES HAVE MORE C
  - PROVIDE SHUNT C (AND SOME SERIES L)

LC REPRESENTATION OF A SHORT LINE



$$X_L = Z_0 \bullet Sin(\beta l)$$

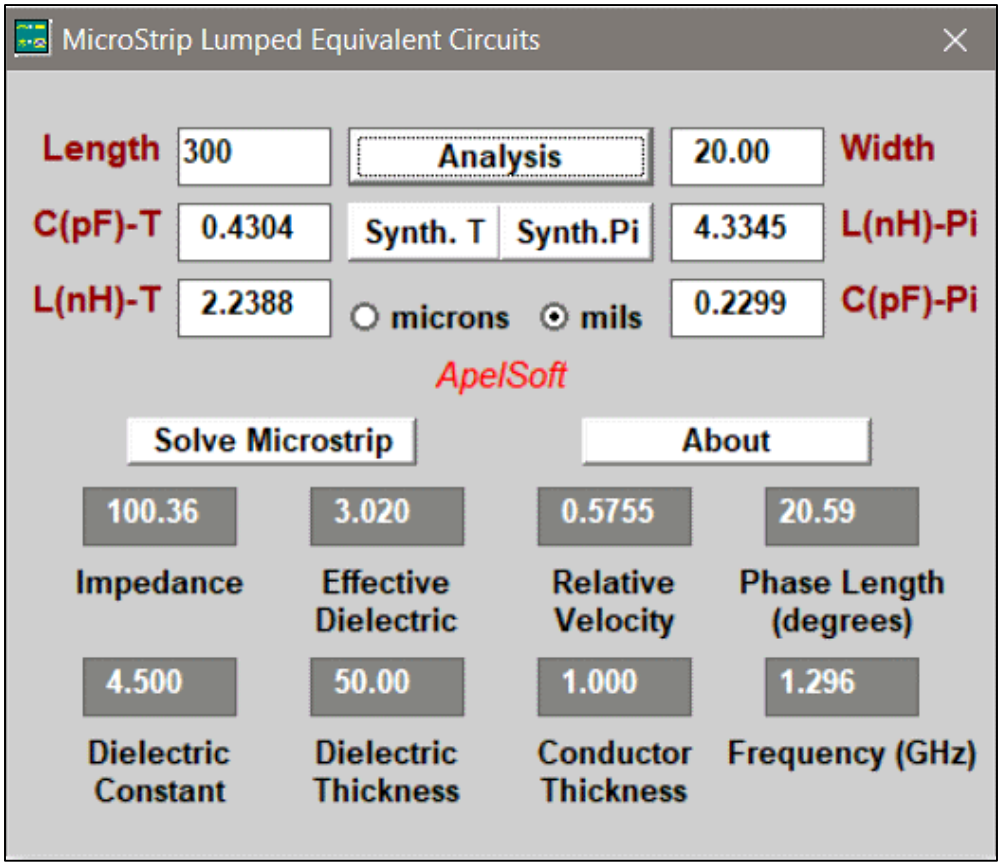
$$X_C = Z_0 \bullet Cot(\beta l/2)$$

$$X_L = Z_0 \bullet Tan(\beta l/2)$$

$$X_C = \frac{Z_0}{Sin(\beta l)}$$

- HIGH Zo LINES USE THE π CIRCUIT FOR INDUCTOR REPRESENTATION
- THE END CAPACITANCES ARE SMALL WITH HIGH Zo LINES
- LOW Zo LINES USE THE T CIRCUIT FOR CAPACITOR REPRESENTATION
- THE END INDUCTANCES ARE SMALL WITH LOW Zo LINES

LUMPED EQUIVALENT CALCULATOR



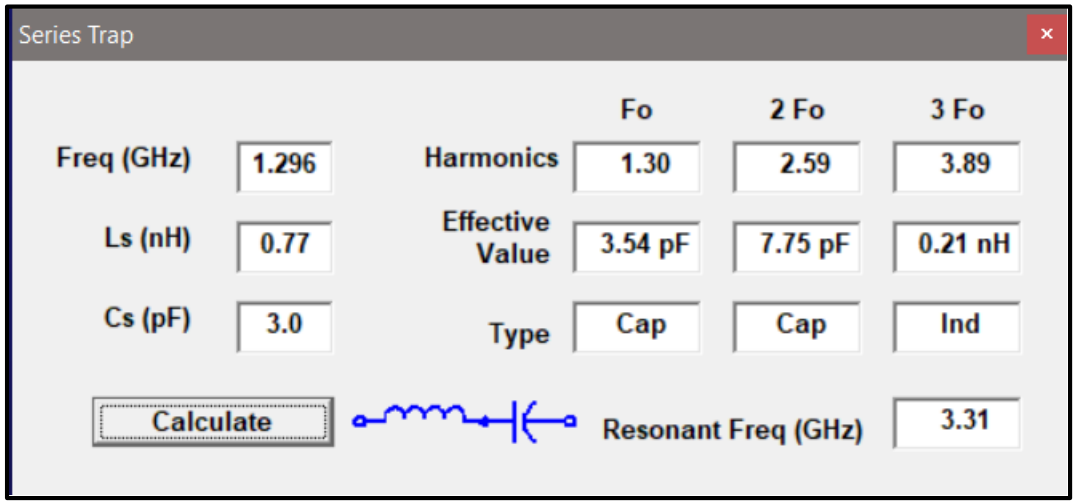
- MICROSTRIP ANALYSIS AND SYNTHESIS
- π and T EQUIVALENT CIRCUIT CALCULATION
- SELECTABLE UNITS: MILS OR MICRONS

http://k5tra.net/TechFiles/LumpEquiv.exe

SMD CHIP SERIES INDUCTANCE

SMD SERIES INDUCTANCE

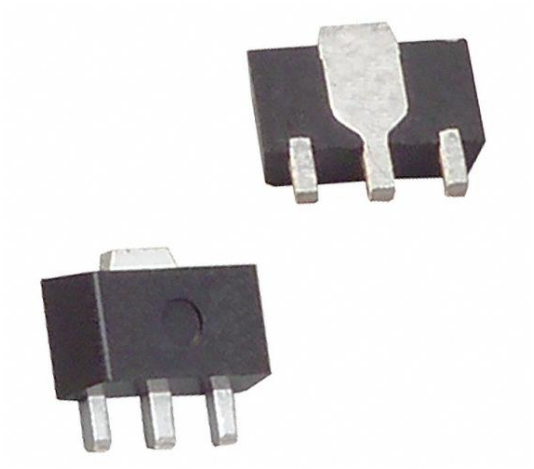
CHIP PKG	DIM (mil^2)	L(nH)
0402	40x20	0.59
0603	60x30	0.77
0805	80x50	0.84
ATC 100A	55x55	0.55
ATC 100B	110x110	0.77

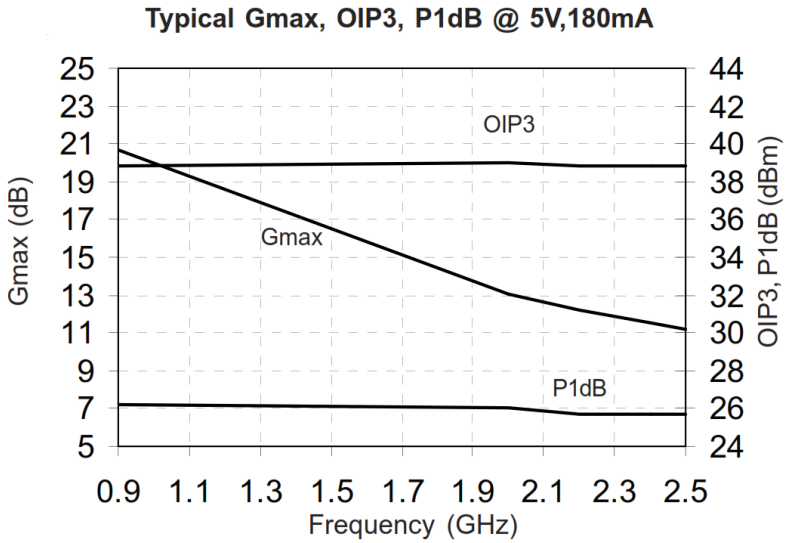


http://k5tra.net/TechFiles/SeriesTrap.exe

- AN 0603 3 pF CAP ALSO HAS 0.77 nH SERIES INDUCTANCE
- SERIES RESONANT FREQUENCY IS 3.31 GHz
- EFFECTIVE CAPACITANCE IS 3.54 AT 1296 MHz
- EFFECTIVE CAPACITANCE IS 7.75 AT 2nd HARMONIC OF 1296 MHz
- EFFECTIVE INDUCTANCE IS 0.21 nH AT 3rd HARMONIC OF 1296 MHz

DESIGN EXAMPLE: SGA-9189 PA DRIVER





- THE SGA-9189 IS A MEDIUM POWER SiGe TRANSISTOR
- > 25 dBm POWER OUTPUT AT Vcc = +5V
- SOT-89 PACKAGE
- MANUFACTURER: RFMD

SGA-9189 TARGET IMPEDANCES

- OPTIMUM EXTERNAL IMPEDANCES:

  $Z_{S\ OPT} = 7.1 - j\ 4.4\ \Omega$

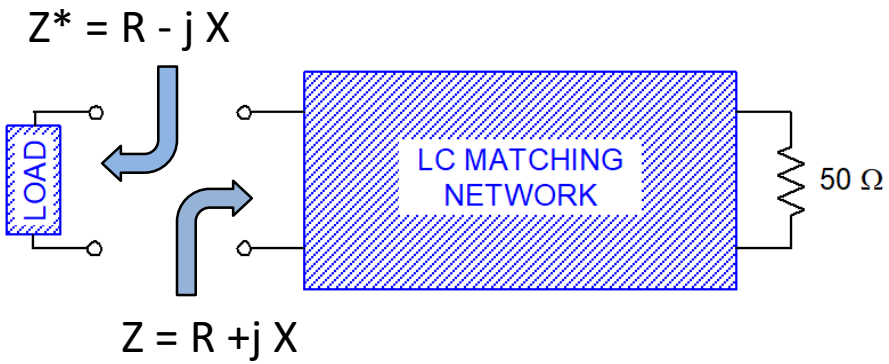
  $Z_{L\ OPT} = 18.4 + j\ 4.1\ \Omega$

- OPTIMUM MATCHING NETWORKS WILL PROVIDE A MATCH TO LOADS THAT ARE COMPLEX CONJUGATE OF THE OPTIMUMS

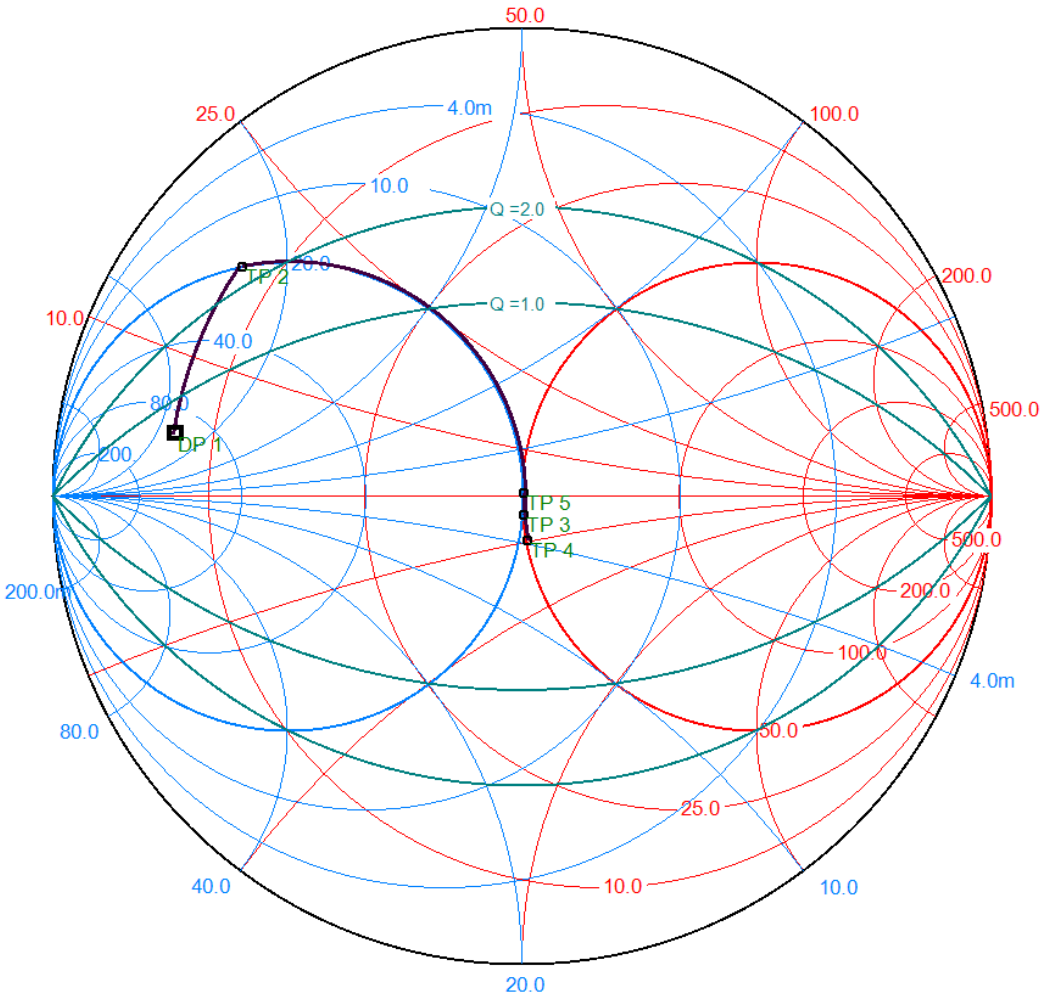
- SO, DESIGN MATCHING NETWORKS TERMINATED WITH:

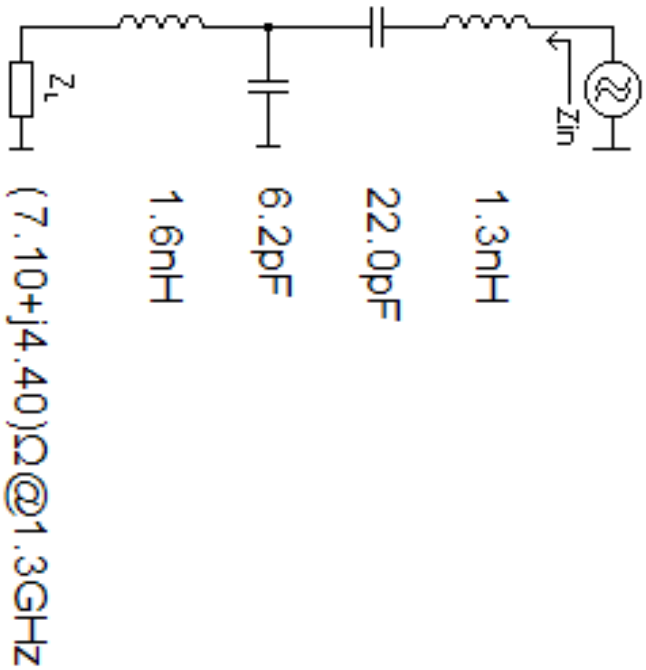
  $Z^*_{S\ OPT} = 7.1 + j\ 4.4\ \Omega$

  $Z^*_{L\ OPT} = 18.4 - j\ 4.1\ \Omega$

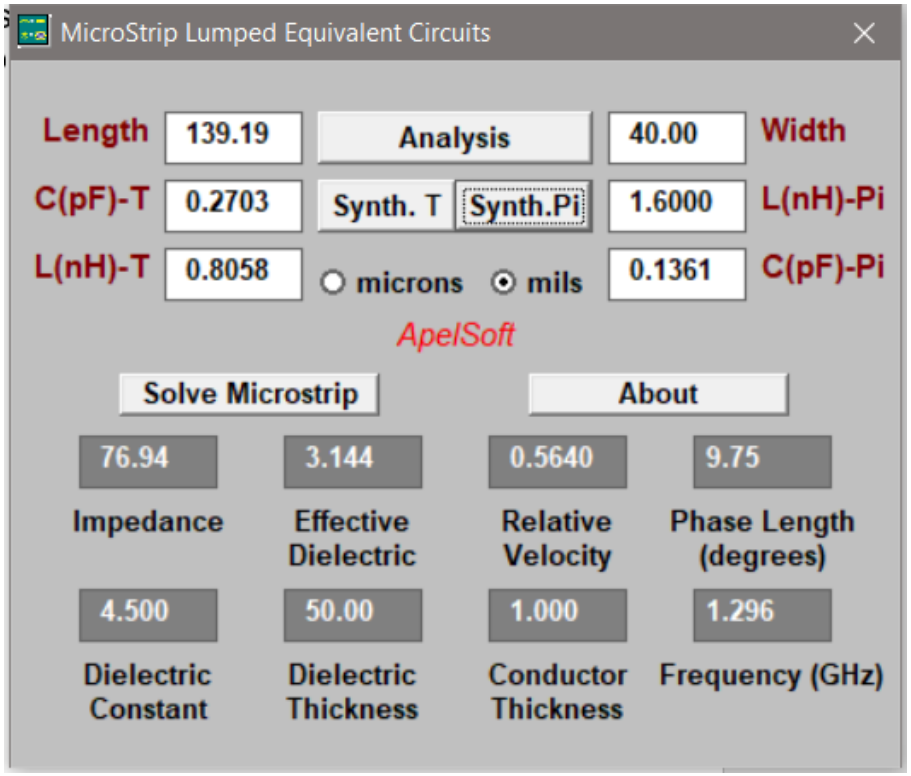


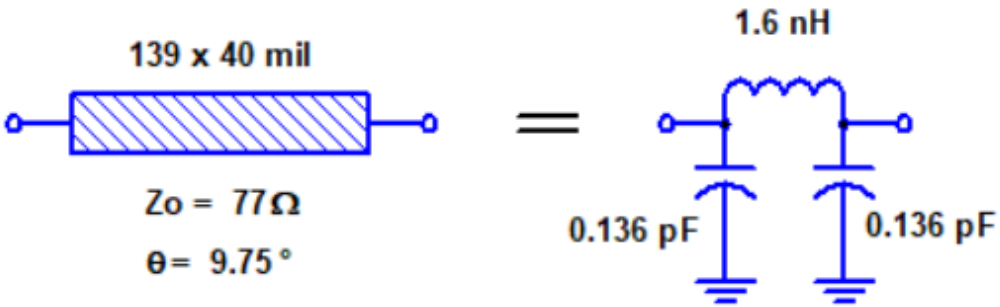
SGA-9189 LC INPUT MATCH





1.6 nH FROM 77 Ω MICROSTRIP

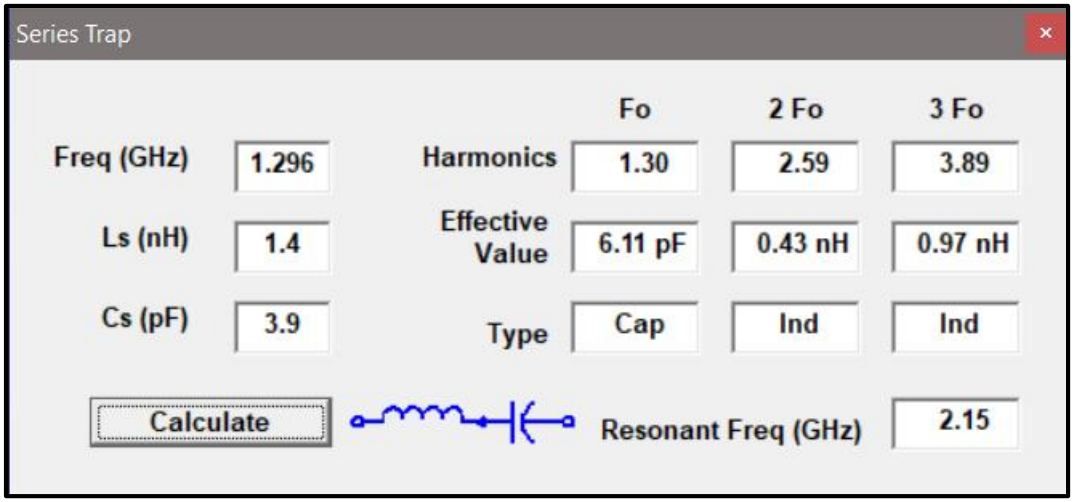




6.2 pF SHUNT CAP

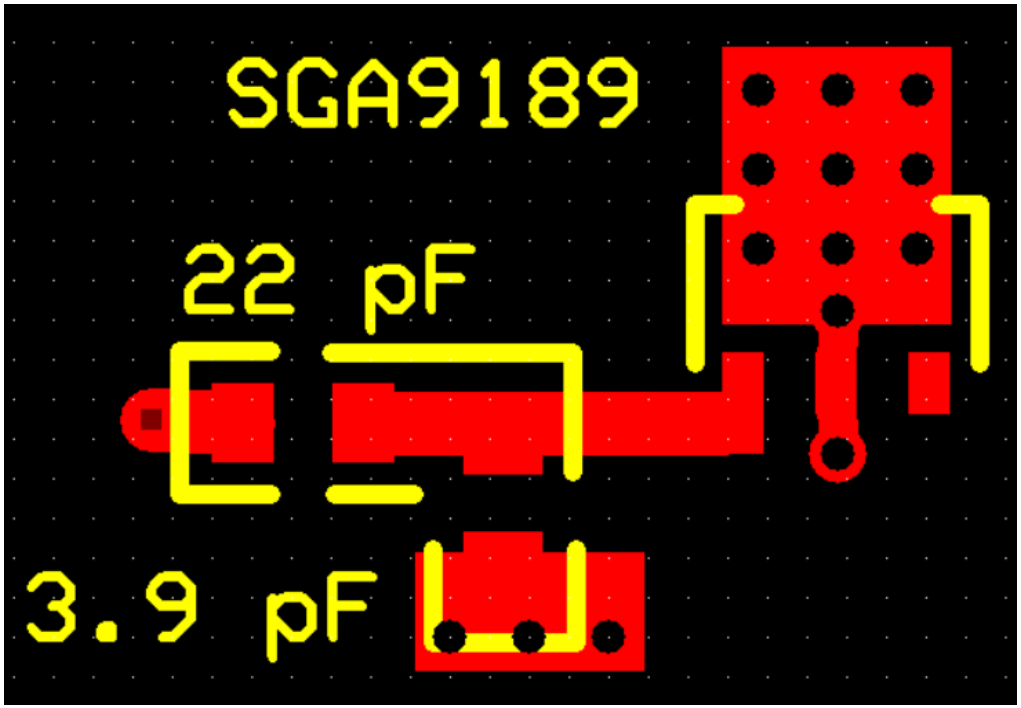
SMD SERIES INDUCTANCE

CHIP PKG	DIM (mil^2)	L(nH)
0402	40x20	0.59
0603	60x30	0.77
0805	80x50	0.84
ATC 100A	55x55	0.55
ATC 100B	110x110	0.77

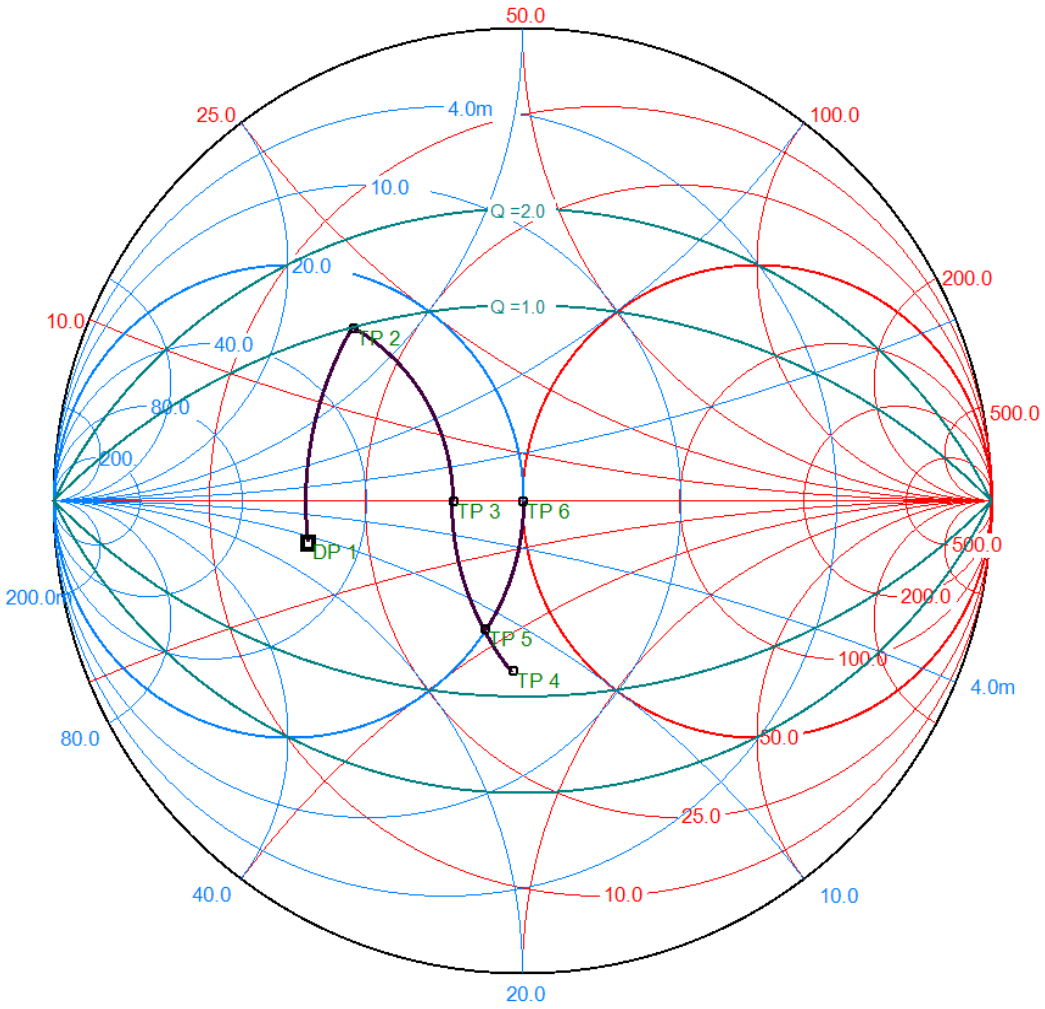


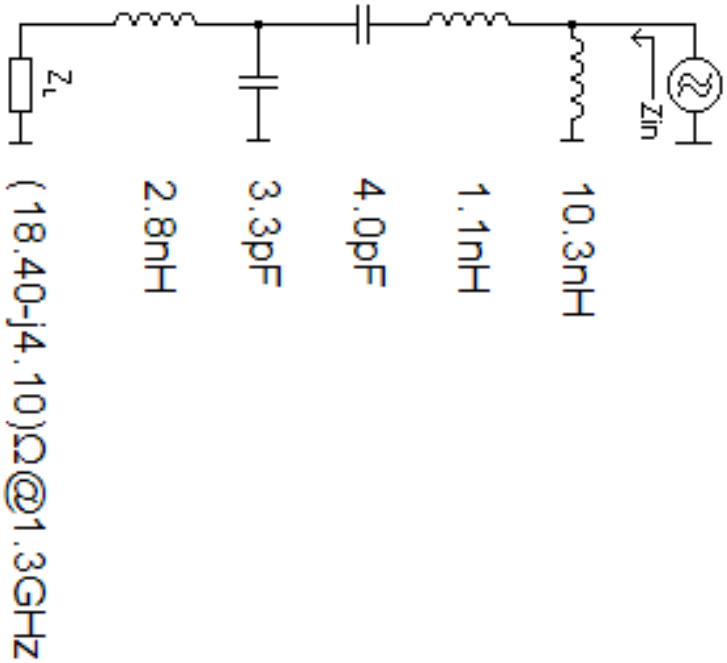
- 0805 SMD 3.9 pF CHIP HAS 0.84 nH IN SERIES
- THE PATH TO GROUND IS A 0.035 DIAMETER VIA = 0.52 nH
- THE TOTAL SERIES INDUCTANCE IS 1.4 nH (= 0.84 + 0.52 nH)
- EFFECTIVE CAPACITANCE IS 6.1 pF AT 1296 MHz
- THE TOTAL SHUNT C IS 6.23 pF (= 6.1 + 0.13 pF)

INPUT MATCH ON 50 MIL FR4

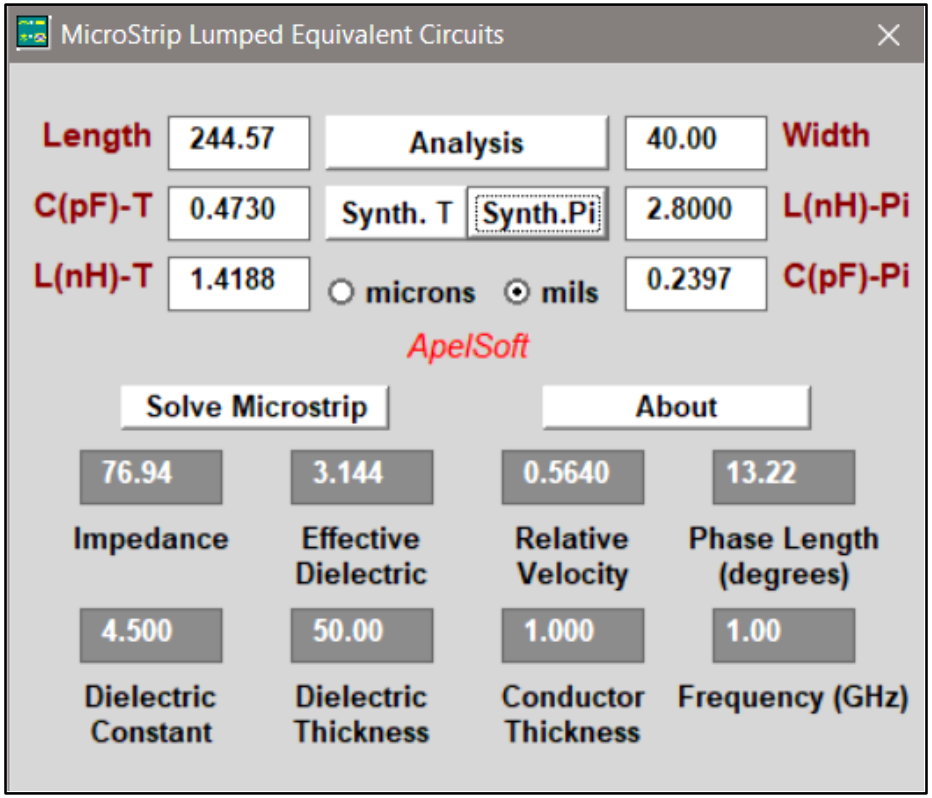


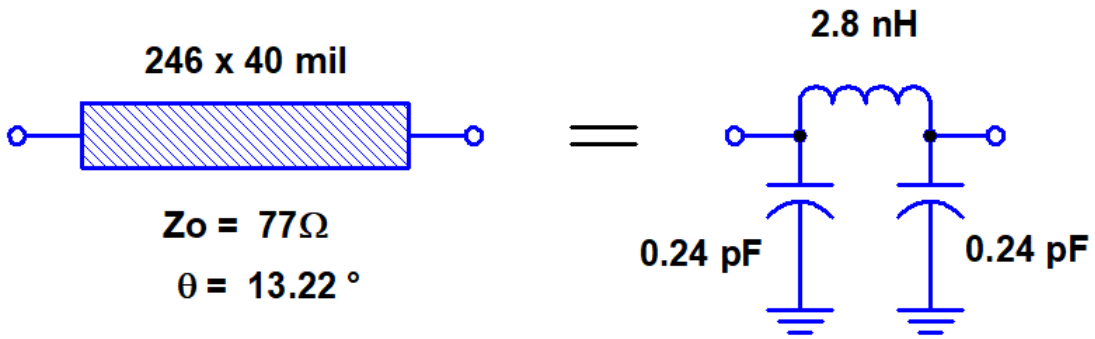
SGA-9189 LC OUTPUT MATCH





2.8 nH FROM 77 Ω MICROSTRIP

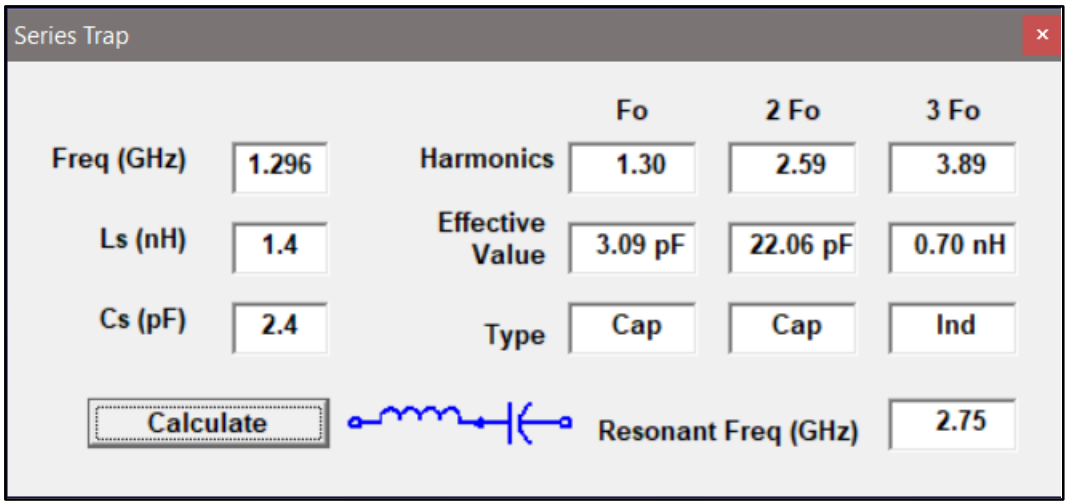




3.3 pF SHUNT CAP

SMD SERIES INDUCTANCE

CHIP PKG	DIM (mil^2)	L(nH)
0402	40x20	0.59
0603	60x30	0.77
0805	80x50	0.84
ATC 100A	55x55	0.55
ATC 100B	110x110	0.77

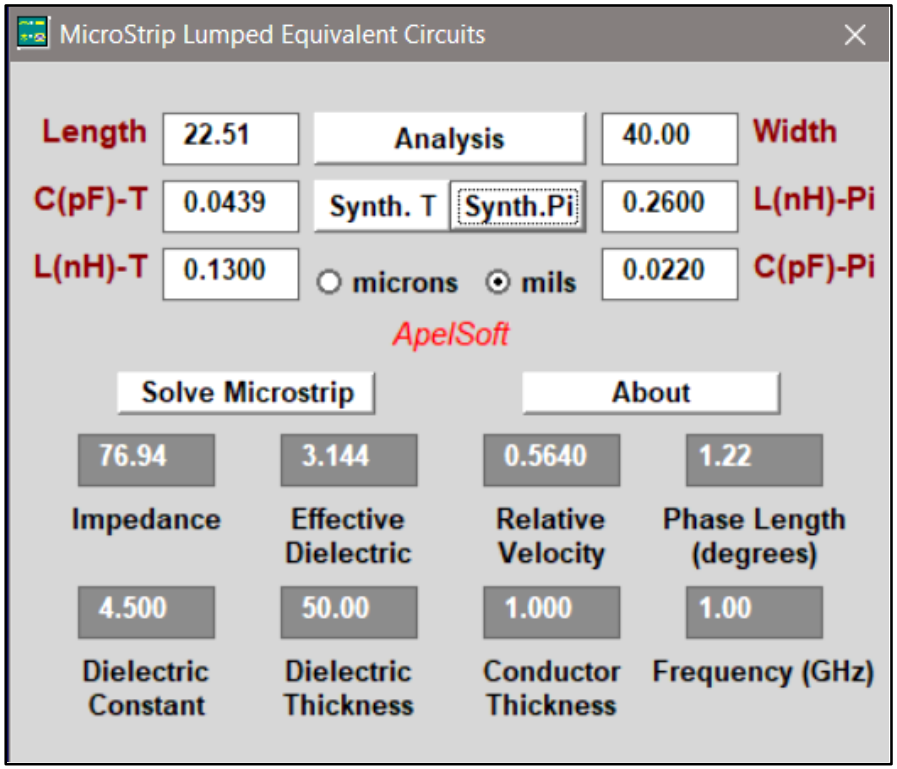


- 0805 SMD 2.4 pF CHIP HAS 0.84 nH IN SERIES
- THE PATH TO GROUND IS A 0.035 DIAMETER VIA = 0.52 nH
- THE TOTAL SERIES INDUCTANCE IS 1.4 nH (= 0.84 + 0.52 nH)
- EFFECTIVE CAPACITANCE IS 3.09 pF AT 1296 MHz
- THE TOTAL SHUNT C IS 3.3 pF (= 3.09 + 0.24 pF)

4.0 pF SERIES CAP

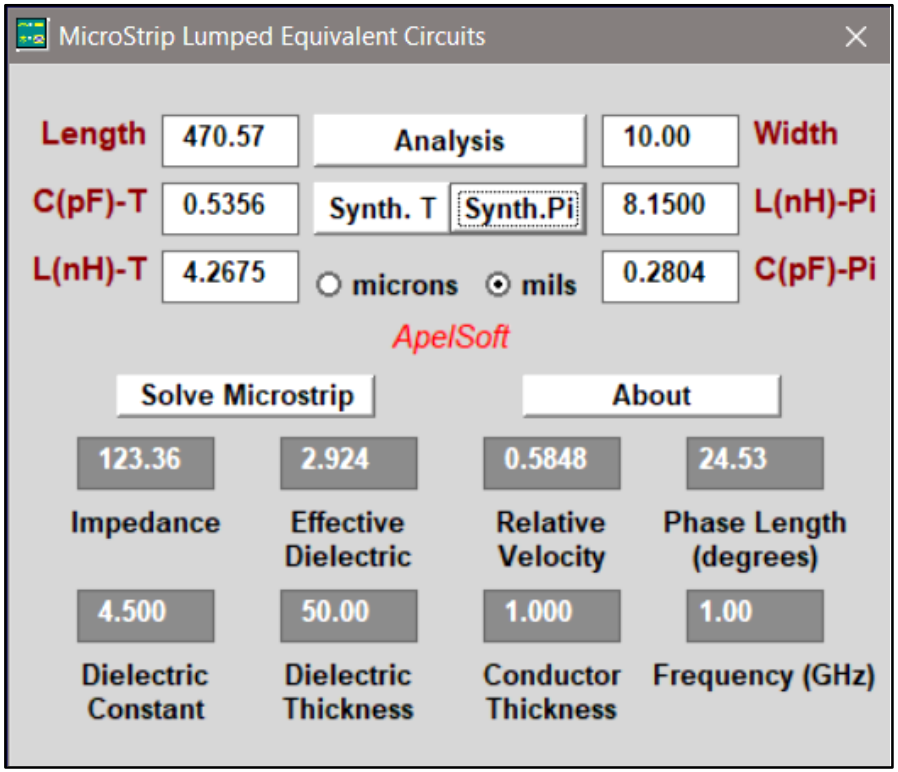
SMD SERIES INDUCTANCE

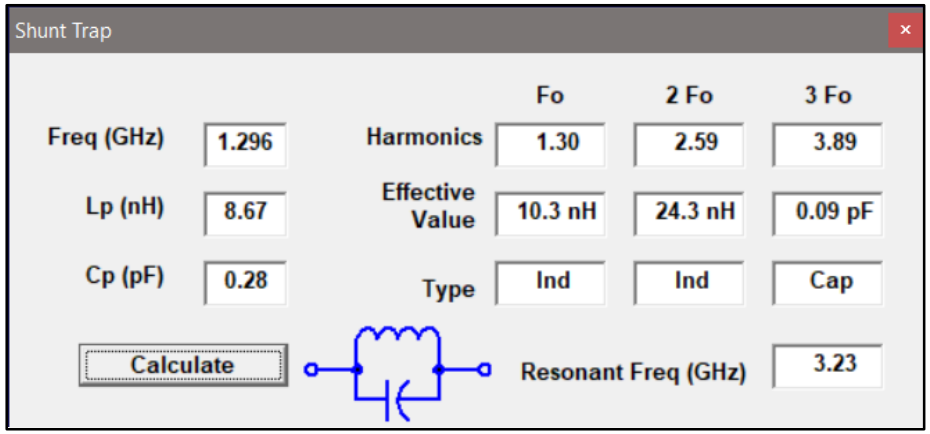
CHIP PKG	DIM (mil^2)	L(nH)
0402	40x20	0.59
0603	60x30	0.77
0805	80x50	0.84
ATC 100A	55x55	0.55
ATC 100B	110x110	0.77



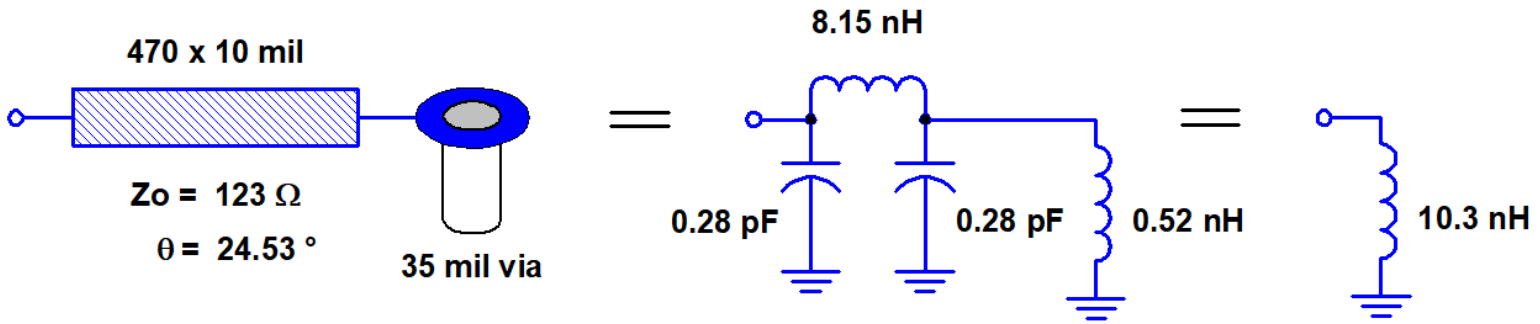
- 0805 SMD 4 pF CHIP HAS 0.84 nH IN SERIES
- THE LUMPED DESIGN HAS PROVIDED 1.1 nH IN SERIES WITH 4 pF
- THE EXCESS 0.26 nH (=1.1 – 0.84 nH) REPRESENTS 22 MILS of 77 Ω LINE

10.3 nH SHUNT INDUCTOR

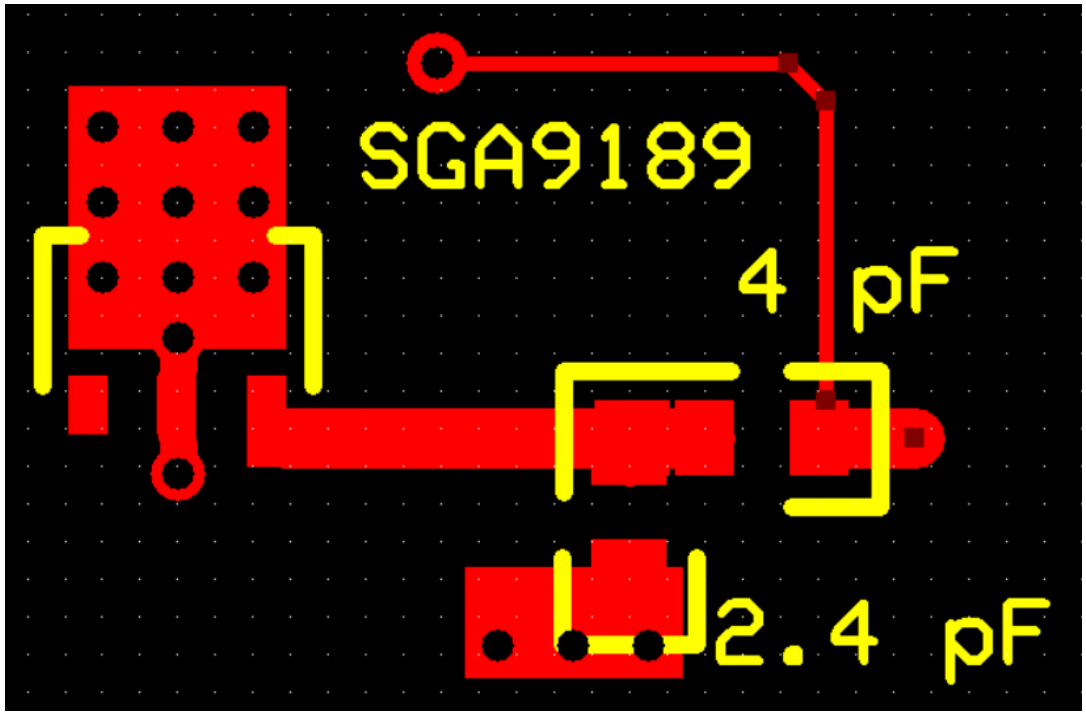




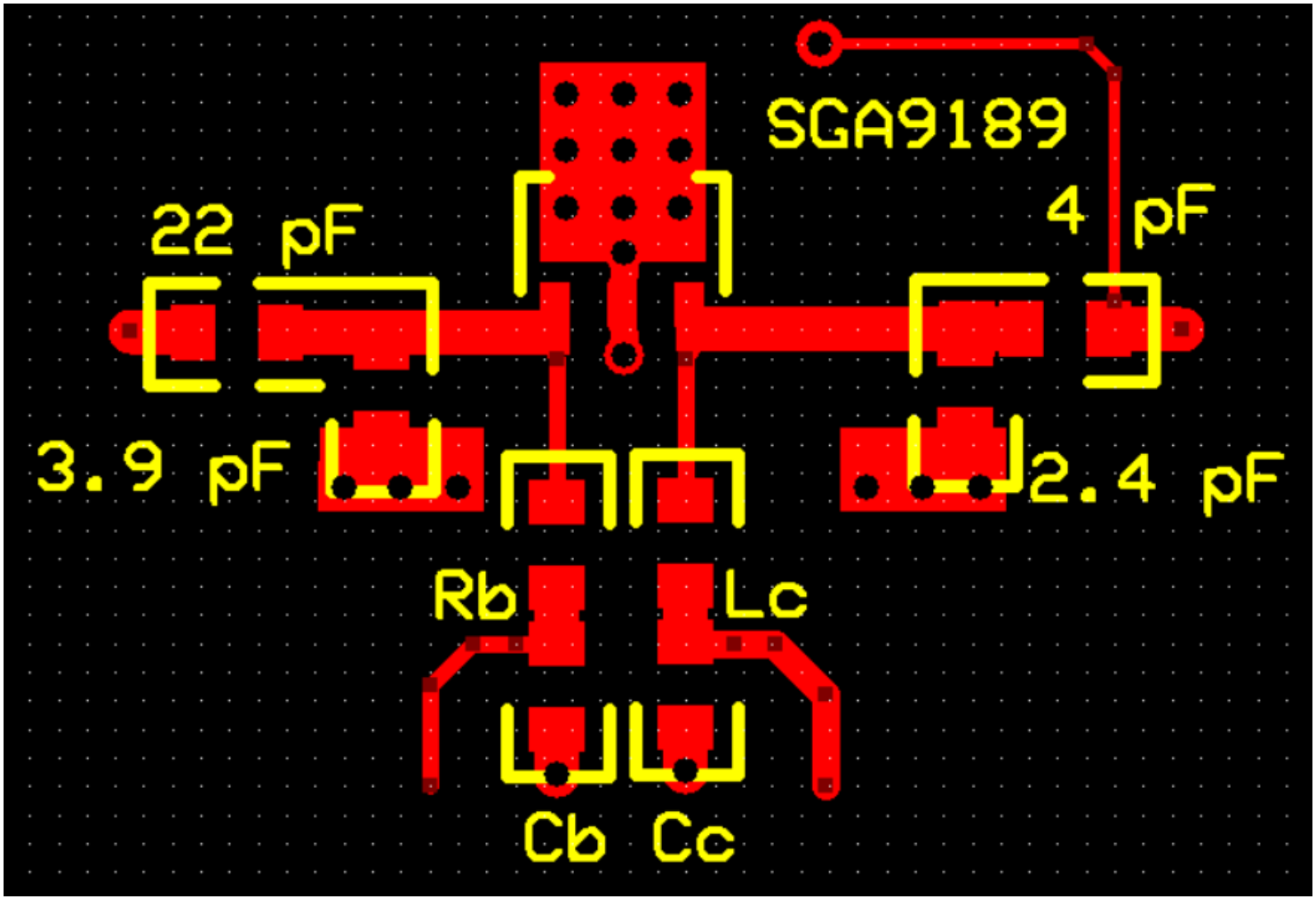
- SHUNT INDUCTOR
- PARALLEL LC EQUIVALENT
- EFFECTIVE INDUCTNCE = 10.3 nH



OUTPUT MATCH ON 50 MIL FR4



1296 MHz DRIVER LAYOUT WITH BIAS FEEDS



SOFTWARE TOOLS

- SMITH:
  http://www.fritz.dellsperger.net/smith.html
- MICROSTRIP LUMPED EQUIVALENT:
  http://k5tra.net/TechFiles/LumpEquiv.exe
- SERIES TRAP:
  http://k5tra.net/TechFiles/SeriesTrap.exe
- SHUNT TRAP:
  http://k5tra.net/TechFiles/ShuntTrap.exe